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AMENDMENTS TO THE CLAIMS:

Please amend claims 4 and 17 as follows:

- 1. 3. (Canceled)
- 4. (Currently Amended) A method of forming metal wires, comprising the steps of:
- a) forming a low-dielectric insulating film on a silicon substrate for which given processes are implemented, and then forming a trench in the low-dielectric insulating film;
 - b) forming lower metal wires within the trench;
- c) adhering a plate in which a plurality of implantation holes are formed and a sidewall of a given height is formed at its edge, an engraved pattern for forming a plurality of trenches formed on the plate, and an engraved pattern for forming a plurality of via holes formed on the engraved pattern for forming the trench, onto a silicon substrate;
- d) implanting injecting a low-dielectric insulating material of a liquid state or a sol or gel state completely into a space through the implantation holes and then annealing the low-dielectric insulating material;
- e) removing the plate to obtain a low-dielectric insulating film pattern having the plurality of the trenches shaped by the engraved pattern for forming the trenches and the plurality of the via holes shaped by the engraved pattern for forming the via holes; and
- f) forming upper metal wires, which are connected to the lower metal wires through the via holes, within the trenches.
- 5. (Original) The method as claimed in claim 4, further comprising the step of forming an anti-diffusion film on the surface of the lower metal wires from the step b).

- 6. (Previously Presented) The method as claimed in claim 5, wherein the anti-diffusion film is made of a metal of a high melting point or a compound that contains Ni, Co, P or B, and is formed by a selective electroless plating method.
- 7. (Original) The method as claimed in claim 4, wherein in the step d), the silicon substrate and the plate are kept at a temperature of $100 \sim 450 \, \text{C}$.
- 8. (Original) The method as claimed in claim 4, wherein the low-dielectric insulating material is made of a material containing carbon or an organic or inorganic series material of a low density and is implanted in thickness of 3000 ~ 30000 Å.
- 9. (Original) The method as claimed in claim 4, wherein the annealing process is implemented for 10seconds ~ 10minutes.
- 10. (Original) The method as claimed in claim 4, further comprising the step of forming an anti-diffusion film on the surface of the upper metal wires from the step f).
- 11. (Original) The method as claimed in claim 4, wherein the upper and lower metal wires consist of an anti-diffusion film and a copper film, and is formed by a damascene process.
- 12. (Original) The method as claimed in claim 11, wherein the anti-diffusion film is made of Ta, TaN, TiN, TiNSi, WN, WCN, or an alloy of their combination, and is formed by a physical vapor deposition method, a chemical vapor deposition method or an atomic layer deposition method.

13. (Original) The method as claimed in claim 11, wherein the copper film is formed by electroplating, electroless plating or chemical vapor deposition method.

14. - 16. (Canceled)

- 17. (Currently Amended) A method of forming metal wires, comprising the steps of:
- a) forming a low-dielectric insulating film on a silicon substrate for which given processes are implemented and then forming a trench in the low-dielectric insulating film;
 - b) forming lower metal wires within the trench;
- c) adhering a plate in which a plurality of first and second implantation holes are each formed and a sidewall of a given height is formed at its edge, an engraved pattern for forming a plurality of trenches formed on the plate, and an engraved pattern for forming a plurality of via holes formed on the engraved pattern for forming the trench, onto a silicon substrate;
- d) implanting injecting a first insulating material of a liquid state or a sol or gel state of a given amount through the first implantation hole and then performing a first annealing process;
- e) implanting injecting a second insulating material of a liquid state or a sol or gel state through the second implantation hole and then performing a second annealing process;
- f) removing the plate to obtain an insulating film pattern of a multi-layer structure having the plurality of the trenches shaped by the engraved pattern for forming the trenches and the plurality of the via holes shaped by the engraved pattern for forming the via holes; and

- g) forming upper metal wires, which are connected to the lower metal wires through the via holes, within the trenches.
- 18. (Original) The method as claimed in claim 17, wherein the second insulating material is made of an inorganic series material having a dielectric of $2.0 \sim 4.5$ capable of serving as an anti-polishing layer.
- 19. (Previously Presented) The method as claimed in claim 17, wherein the first annealing process in the step d) is implemented for 10 seconds ~ 10 minutes under an inert gas atmosphere of over 1 atmospheric pressure
- 20. (Previously Presented) The method as claimed in claim 17, wherein the second annealing process in the step e) is implemented for 10 seconds ~ 10 minutes under an inert gas atmosphere of over 1 atmospheric pressure.